



## Si9166 Demonstration Board

### FEATURES

- Voltage Mode Control
- 2.7- to 6-V Input Voltage Rang for  $V_{DD}$  and  $V_S$
- Programmable PWM/PSM Control
- Up to 2-MHz Switching Frequency in PWM
- Synchronous Rectification in PWM
- Less Than 200- $\mu$ A  $I_{DD}$  in PSM
- Integrated UVLO and POR
- Integrated Soft-Start
- Synchronization
- Shutdown Current  $< 1 \mu$ A
- Wide Bandwidth Feedback Amplifier
- Single-Cell Li+ and 3-Cell NiCd or NiMH Operation

### DESCRIPTION

The Si9166 controller is based on Si9165 design without internal MOSFETs, so higher power level can be achieved by properly choosing external MOSFETs, making it the optimum choice of RF power amplifier for cellular phone applications. This demo board uses Si6801 dual MOSFET and can be easily upgraded to higher current MOSFET Si6803 without changing the layout. The Si6801 is optimum for peak drain current of 1.5 to 1.9 A, while Si6803 is suitable for 2- to 2.5-A peak drain current.

There are two different version of demo boards (DB), buck and boost converters, because the Si9166 can be easily configured to buck or boost modes.

The demo board has been configured to generate 2.7-V regulated output for buck DB while for boost DB is 3.6 V. The output voltage set point of boost converter can be easily adjusted by changing the value of  $R_2$  (See Figure 2) using the formula

$$R_2 = \frac{R_1}{\frac{V_{OUT}}{V_{REF}} - 1} \quad (1)$$

The typical value of  $V_{REF}$  is 1.3 V. The reference designator used for buck DB is  $R_2$  and  $R_4$  instead of  $R_1$  and  $R_2$ , respectively. It is recommended not to change  $R_1$  since that would alter the control loop compensation.

The PWM/PSM pin can be used to program the controller to operate in PWM or PSM mode. PWM is normal pulse width modulation to keep output regulated through out the load range, while the PSM mode offers better efficiency at light load to conserve power by skipping switching pulses. Notice the PSM only gain efficiency advantage at light load and can only deliver certain load current (about 150 mA) before output drops out of regulation.

Included in this document are schematics (Figure 1 and 2), demo board sample waveform (Figure 3 through 6), PCB layout (Figure 7 through 12), and Bill Of Material (Table 1 and 2).

*The demonstration board layout is available in Gerber file format. Please contact your Vishay Siliconix sales representative or distributor for a copy.*

### ORDERING INFORMATION: PART NUMBER

**Si9166DB-K (BUCK CONVERTER)**  
**Si9166DB-S (BOOST CONVERTER)**

### TEST SETUP AND OPERATION

1. Visually inspect demo board and make sure that Jumper 1 is set to PWM and Jumper 2 is set to Enable.
2. Attach an electronic load set to either resistive or current mode to the output pins (P3 and P4) on the demo board. Set the load current to 200 mA or equivalent resistor value. After the converter is powered up, output load current can be adjusted.
3. Attach a dc power supply, with at least 3-A current capability, to the input pins (P1 and P2) on the demo board. The input voltage can be adjusted between 2.7 and 3.6 V for boost DB or 2.7 to 6 V for buck DB.
4. Put an oscilloscope ground on the input ground, and the Ch1 probe on pin 8 of Si6801 (the MOSFET drain). Connect Ch2 probe on pin 3 of Si9166 (DH) and Ch3 on pin 14 (DL). The waveform for buck and boost DB should appear approximately as shown in Figure 2 and 3, respectively.
5. To test your DB in PSM, adjust the load to 20 mA. Then change Jumper 1 setting to PSM. Notice the reduction of the input current. With the same probe setup mentioned above, the waveform for buck and boost DB should appear approximately as shown in Figure 4 and 5, respectively.

### SCHEMATIC DIAGRAMS

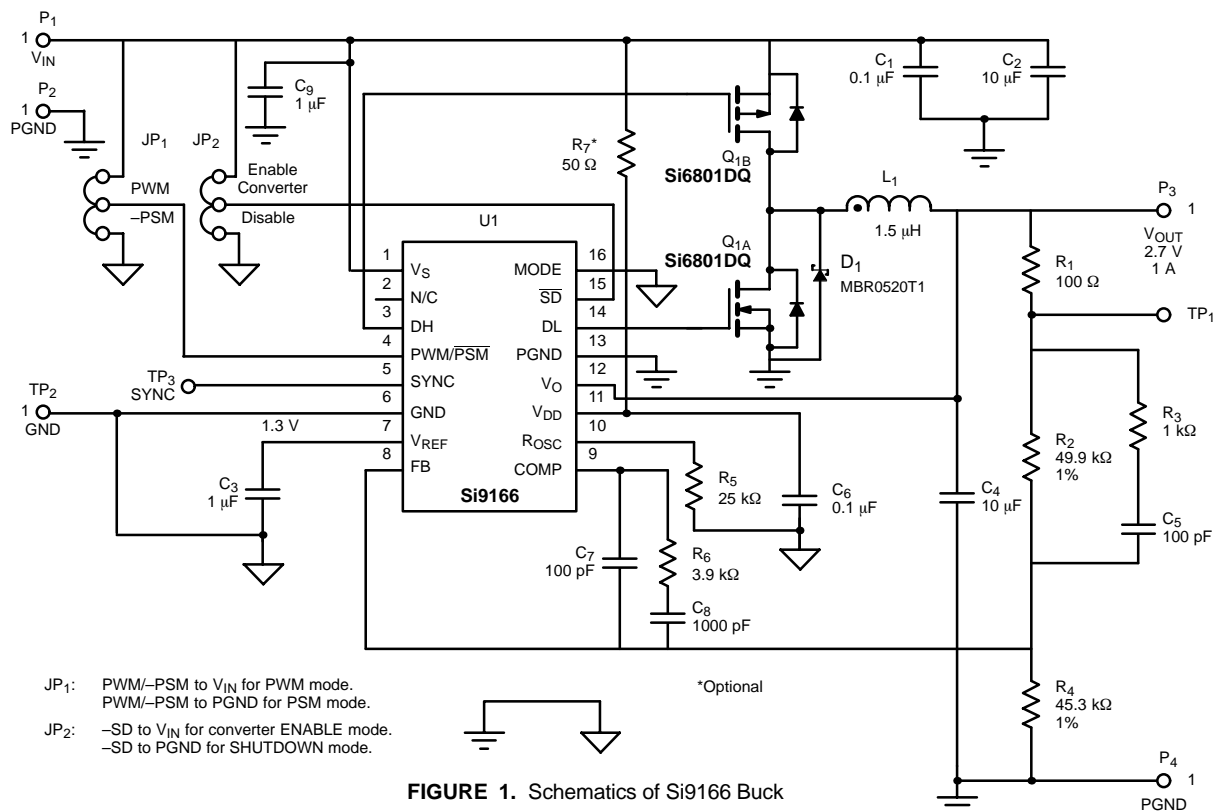


FIGURE 1. Schematics of Si9166 Buck

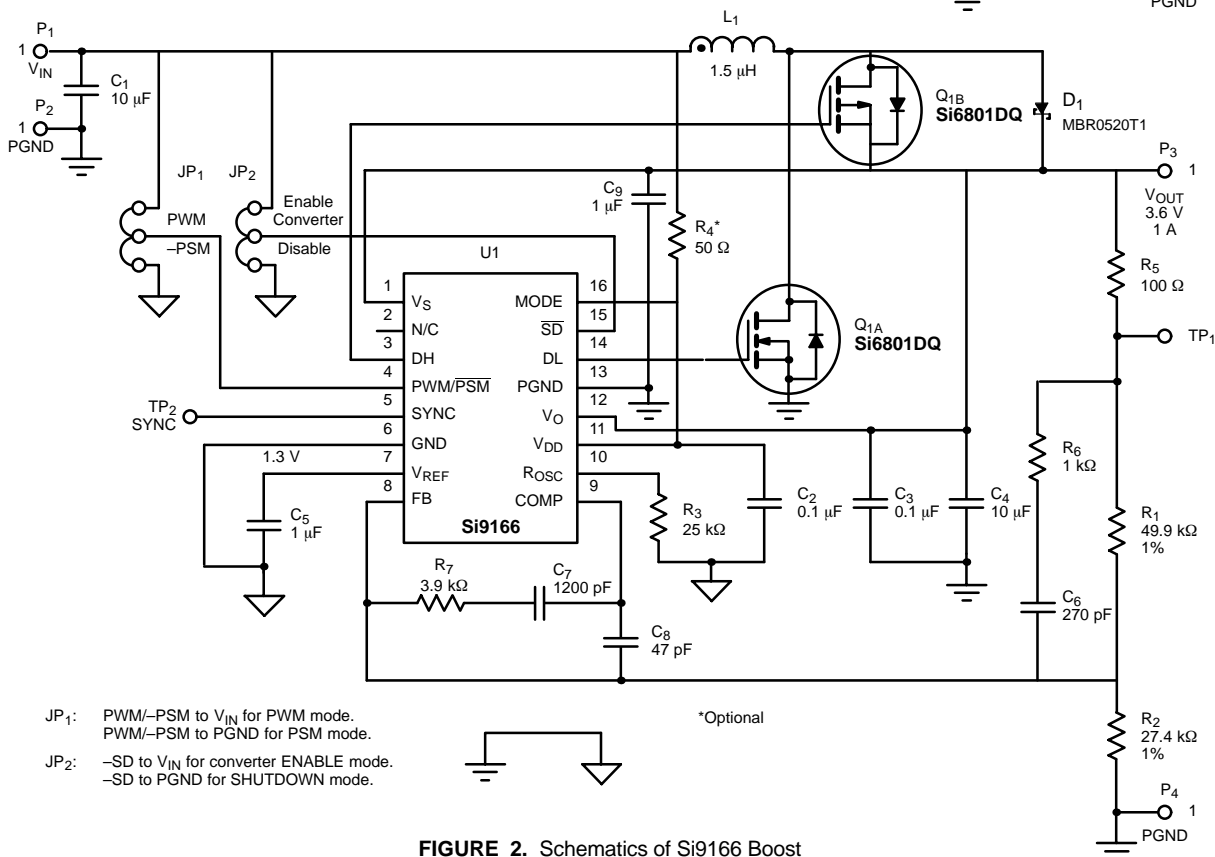
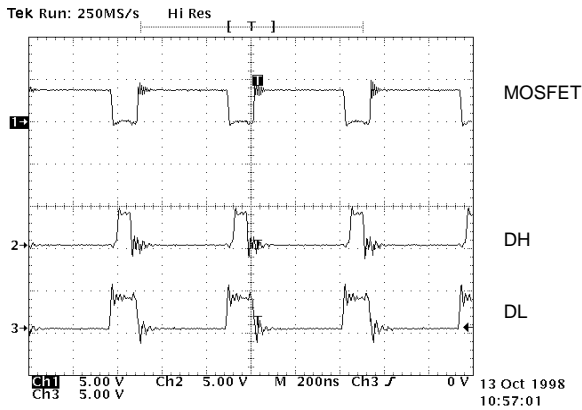


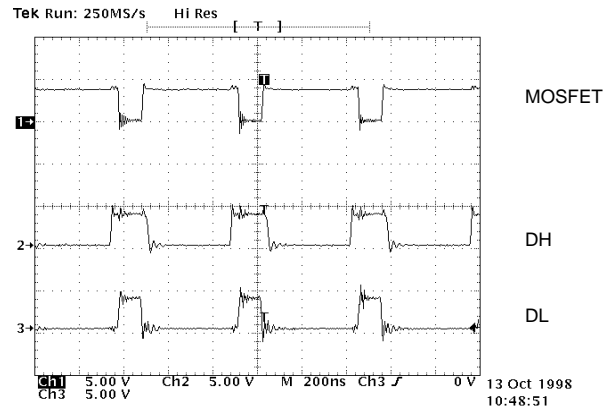
FIGURE 2. Schematics of Si9166 Boost

**CHANNEL LINEUP FOR FIGURES 3 THROUGH 6**

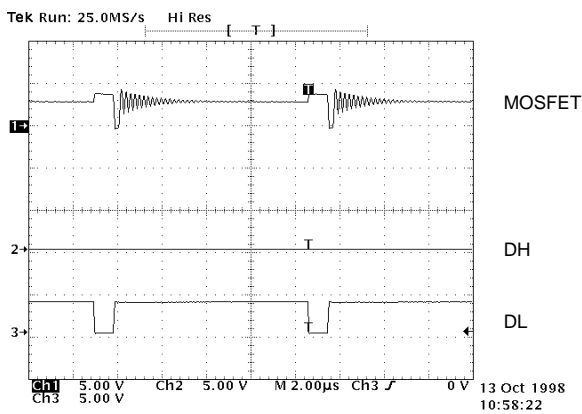
Ch1: Drain Voltage of MOSFET (Pins 1 and 8)  
 Ch2: High-Side Switch Drive (Pin 3)  
 Ch3: Low-Side Switch Drive (Pin 14)



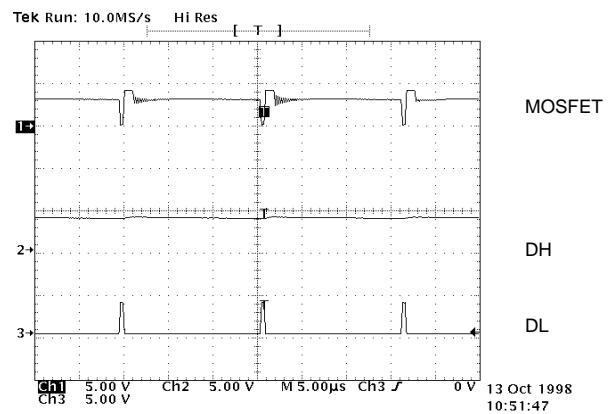
**FIGURE 3.** Buck DB PWM Mode:  $V_{IN} = 3.6\text{ V}$ ,  $V_{OUT} = 2.7\text{ V}$ , Load = 200 mA



**FIGURE 4.** Boost DB PWM Mode:  $V_{IN} = 3\text{ V}$ ,  $V_{OUT} = 3.6\text{ V}$ , Load = 200 mA



**FIGURE 5.** Buck DB PSM Mode:  $V_{IN} = 3.6\text{ V}$ ,  $V_{OUT} = 2.7\text{ V}$ , Load = 20 mA



**FIGURE 6.** Boost DB PSM Mode:  $V_{IN} = 3\text{ V}$ ,  $V_{OUT} = 3.6\text{ V}$ , Load = 20 mA

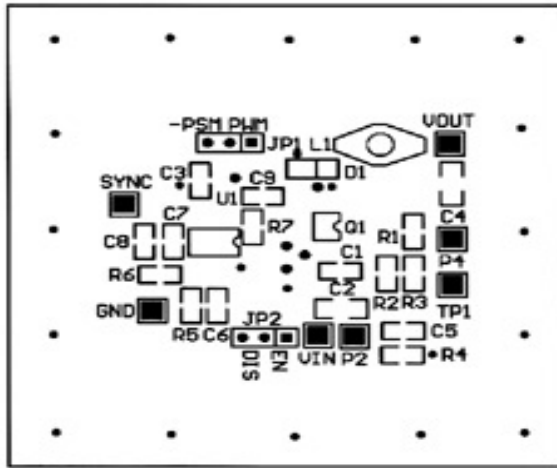


FIGURE 7. Buck—Top Silk Screen

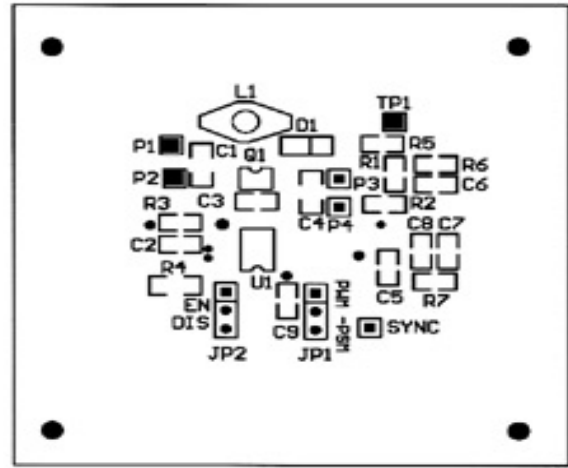


FIGURE 10. Boost—Top Silk Screen

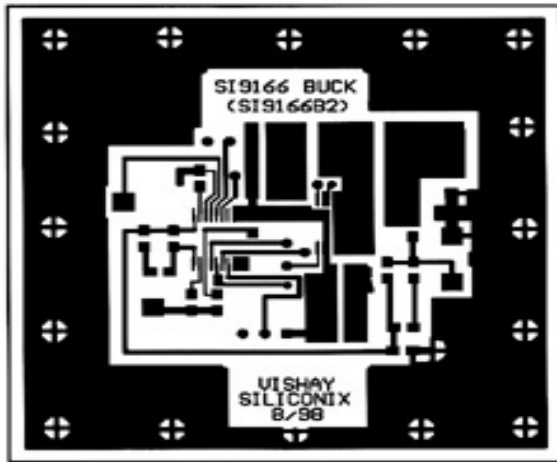


FIGURE 8. Buck—Top Layer

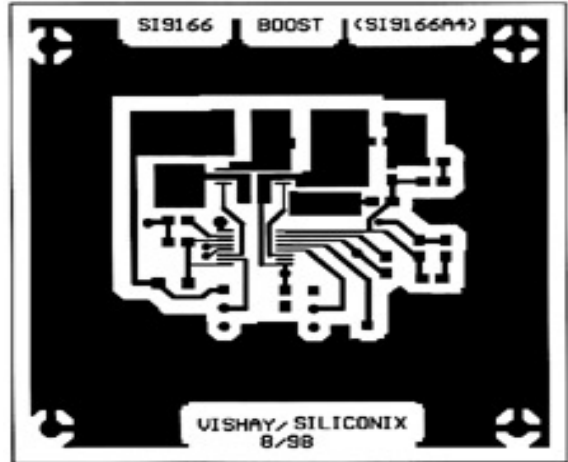


FIGURE 11. Boost—Top Layer

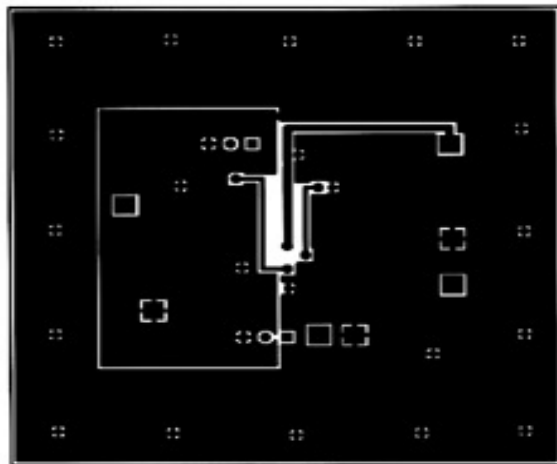


FIGURE 9. Buck—Bottom Layer

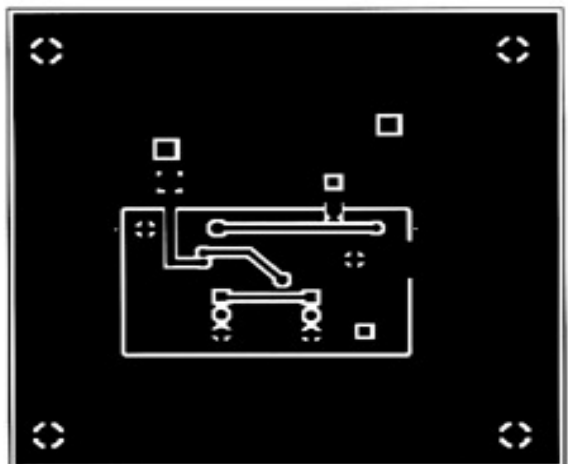


FIGURE 12. Boost—Bottom Layer



**TABLE 1. BUCK DEMO BOARD BILL-OF-MATERIAL**

Item	Qty	Designator	Part Type	Description	Footprint	Part Number	Manufacturer
1	1	R <sub>1</sub>	100 Ω	Resistor, 1%, 1/8 W	0805	CRCW08051000FRT1	Vishay Dale
2	1	R <sub>2</sub>	49.9 kΩ	Resistor, 1%, 1/8 W	0805	CRCW08054992FRT1	Vishay Dale
3	1	R <sub>3</sub>	1 kΩ	Resistor, 5%, 1/8 W	0805	CRCW0805102JRT1	Vishay Dale
4	1	R <sub>4</sub>	45.3 kΩ	Resistor, 1%, 1/8 W	0805	CRCW08054532FRT1	Vishay Dale
5	1	R <sub>5</sub>	25 kΩ	Resistor, 5%, 1/8 W	0805	CRCW0805253JRT1	Vishay Dale
6	1	R <sub>6</sub>	3.9 kΩ	Resistor, 1%, 1/8 W	0805	CRCW08053901FRT1	Vishay Dale
7	1	R <sub>7</sub>	50 Ω	Resistor, 5%, 1/8 W	0805	CRCW0805500JRT1	Vishay Dale
8	2	C <sub>1</sub> , C <sub>6</sub>	0.1 μF	Capacitor, Ceramic	0805	VJ0805104KXXAT	Vishay Vitramon
9	2	C <sub>2</sub> , C <sub>4</sub>	10 μF	Capacitor, Ceramic, 10 V	1206	GRM42-2X5R106K16	Murata
10	2	C <sub>3</sub> , C <sub>9</sub>	1 μF	Capacitor, Ceramic	0805	VJ0805105KXXAT	Vishay Vitramon
11	2	C <sub>5</sub> , C <sub>7</sub>	100 pF	Capacitor, Ceramic	0805	VJ0805101KXXAT	Vishay Vitramon
12	1	C <sub>8</sub>	1000 pF	Capacitor, Ceramic	0805	VJ0805102KXXAT	Vishay Vitramon
13	1	D <sub>1</sub>	MBR0520T1	Schottky Diode	SOD-123	MBR0520T1	Motorola
14	1	L <sub>1</sub>	1.5 μH	1.5-μH Inductor	IHLP2525	IHLP2525-1-5	Vishay Dale
15	1	U <sub>1</sub>		Power IC	TSSOP-16	Si9166	Vishay Siliconix
16	1	Q <sub>1</sub>		Dual N-/P-Channel MOSFET	TSSOP-8	Si6801DQ	Vishay Siliconix
17	1	JP <sub>1</sub> , JP <sub>2</sub>	Jumpers	3-Pin Jumpers	SIP-3	SIP-3	Multi-Source
18	4	P <sub>1</sub> to P <sub>4</sub>	Power GND	1-Pin Header	TP <sub>1</sub>	TP <sub>1</sub>	Multi-Source
19	3	P <sub>1</sub> to P <sub>4</sub>	Test Point	1-Pin Header	TP <sub>1</sub>	TP <sub>1</sub>	Multi-Source

**TABLE 2. BOOST DEMO BOARD BILL-OF-MATERIAL**

Item	Qty	Designator	Part Type	Description	Footprint	Part Number	Manufacturer
1	1	R <sub>1</sub>	49.9 kΩ	Resistor, 1%, 1/8 W	0805	CRCW08054992FRT1	Vishay Dale
2	1	R <sub>2</sub>	27.4 kΩ	Resistor, 1%, 1/8 W	0805	CRCW08052742FRT1	Vishay Dale
3	1	R <sub>3</sub>	25 kΩ	Resistor, 5%, 1/8 W	0805	CRCW0805253JRT1	Vishay Dale
4	1	R <sub>4</sub>	50 Ω	Resistor, 5%, 1/8 W	0805	CRCW0805500JRT1	Vishay Dale
5	1	R <sub>5</sub>	100 Ω	Resistor, 5%, 1/8 W	0805	CRCW0805101JRT1	Vishay Dale
6	1	R <sub>6</sub>	1 kΩ	Resistor, 5%, 1/8 W	0805	CRCW0805102JRT1	Vishay Dale
7	1	R <sub>7</sub>	3.9 kΩ	Resistor, 5%, 1/8 W	0805	CRCW0805392JRT1	Vishay Dale
8	2	C <sub>1</sub> , C <sub>4</sub>	10 μF	Capacitor, Ceramic, 10 V	01206	GRM42-2X5R106K16	Murata
9	2	C <sub>2</sub> , C <sub>3</sub>	0.1 μF	Capacitor, Ceramic	0805	VJ0805104KXXAT	Vishay Vitramon
10	2	C <sub>5</sub> , C <sub>9</sub>	1 μF	Capacitor, Ceramic	0805	VJ0805105KXXAT	Vishay Vitramon
11	1	C <sub>6</sub>	270 pF	Capacitor, Ceramic	0805	VJ0805271KXXAT	Vishay Vitramon
12	1	C <sub>7</sub>	1200 pF	Capacitor, Ceramic	0805	VJ0805122KXXAT	Vishay Vitramon
13	1	C <sub>8</sub>	47 pF	Capacitor, Ceramic	0805	VJ0805470KXXAT	Vishay Vitramon
14	1	D <sub>1</sub>	MBR0520T1	Schottky Diode	SOD-123	MBR0520T1	Motorola
15	1	L <sub>1</sub>	1.5 μH	1.5-μH Inductor	IHLP2525	IHLP2525-1-5	Vishay Dale
16	1	U <sub>1</sub>		Power IC	TSSOP-16	Si9166	Vishay Siliconix
17	1	Q <sub>1</sub>		Dual N-/P-Channel MOSFET	TSSOP-8	Si6801DQ	Vishay Siliconix
18	2	JP <sub>1</sub> , JP <sub>2</sub>	Jumpers	3-Pin Jumpers	SIP-3	SIP-3	Multi-Source
19	4	P <sub>1</sub> to P <sub>4</sub>	Power GND	1-Pin Header	TP <sub>1</sub>	TP <sub>1</sub>	Multi-Source
20	2	TP <sub>1</sub> to TP <sub>2</sub>	Test Point	1-Pin Header	TP <sub>1</sub>	TP <sub>1</sub>	Multi-Source